Advance digital design

Hora	Sábado 22	Hora	Lunes	Martes	Miércoles	Jueves	Viernes	Sábado 29
		08:30 a 09:00	Acreditación					
09:30-11:30	Acreditación + Café	09:00 a 11:00	Lab 2: Verilog for simulation (Test Bench)	Design Compiler	IC Compiler Place & Route Flow			
		11:00 a 11:30	Café					
11:30 a 13:00	Introduction to Digital Design Flow	11:30 a 13:00	Simulation of Digital Circuits with VCS	Lab 4: Synthesis with Design Compiler	Lab 6: Place & Route with IC Compiler			
13:00-14:30	Almuerzo	13:00 a 14:30	Almuerzo					
14:30 a 15:40	Verilog Overview	14:30 a 16:00	Lab 3: Simulation with VCS	Design Compiler Topographical	IC Compiler Place & Route			
15:40 a 17:00	Lab 1: Verilog Synthesizable	16:00 a 16:30	Café					
17:00 a 17:30	Café	16:30 a 18:00	Lab 3: Simulation with VCS	Lab 5: Synthesis with Design Compiler Topographical	Lab 7: Place & Route with IC Compiler			
17:30 a 19:00	Lab 1: Verilog Synthesizable	18:00 a 19:00	Plenarias					
19:00 a 21:00	Libre	19:00 a 21:00	Acto Apertura	Lab 5: Synthesis with Design Compiler Topographical	Lab 7: Place & Route with IC Compiler	Cocktail	Cierre	